LESSON PLAN

Subject Code & Name: 16EC2010 & Digital Electronics
Branch: E.C.E-B Class / Semester: II/II Academic Year:2017-18

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective action upon review
		Review of Number Systems:	**I**			
1	**29.11.2017**	Decimal to Binary, Octal, Hexadecimal conversions		Chalk & Board		
2	**30.11.2017**	Binary to Decimal, Octal, Hexadecimal conversions		„		
3	**30.11.2017**	Octal to Decimal, Binary, Hexadecimal conversions		„		
4	**01.12.2017**	Additions in number systems		„		
5	**06.12.2017**	Complements of numbers		„		
6	**07.12.2017**	r's & r-1's complement subtraction		„		
7	**07.12.2017**	BCD codes, Excess 3 codes		„		
8	**08.12.2017**	Alphanumeric codes, self complemented codes, 2421, gray codes		„		
9	**13.12.2017**	Error detection and correction codes		„		
10	**14.12.2017**	Parity checking codes		„		
11	**14.12.2017**	Hamming code		„		
		Logic Operations:	**II**	Chalk & Board		
12	**15.12.2017**	Gates - AND, OR, NOT		„		
13	**20.12.2017**	NAND, NOR, XOR, XNOR		„		
14	**21.12.2017**	Boolean theorems		„		
		Boolean theorems		„		
15	**21.12.2017**	Complements and dual of logic expressions		„		
16	**22.12.2017**	Standard SOP, POS		„		
17	**03.01.2018**	Minimization of logic functions using theorems		„		
18	**04.01.2018**	Minimization of logic functions using theorems		„		
19	**04.01.2018**	Multilevel NAND-NAND realization		„		
20	**05.01.2018**	Multilevel NOR-NOR realization		„		
		Minimisation of switching functions:				
21	**10.01.2018**	Using K-map (2,3 variable)		„		
22	**17.01.2018**	Using K-map (4,5 variable)		„		
23	**18.01.2018**	Using tabular method		„		
24	**18.01.2018**	Code convertors: BCD-excess3, vice-versa		„		
25	**19.01.2018**	Binary-gray, vice-versa		„		
		Combinational Logic Circuits - I	**III**	Chalk & Board		
26	**31.01.2018**	Design of Half &Full Adders		„		
27	**01.02.2018**	Design of Half Subtractor		„		

28	**01.02.2018**	Design of Full Subtractor		„		
29	**02.02.2018**	Design of 4-bit binary adder		„		
30	**07.02.2018**	Design of 4-bit binary subtractor		„		
31	**08.02.2018**	Design of BCD Adder		„		
32	**08.02.2018**	Design of Excess-3 adder		„		
33	**09.02.2018**	Design of carry look ahead adder		„		
		Combinational Logic Circuits - II	**IV**	Chalk & Board		
34	**14.02.2018**	Design of Decoders		„		
35	**15.02.2018**	Design of Encoders		„		
36	**15.02.2018**	Design of higher order decoder and encoder		„		
37	**16.02.2018**	Design of multiplexers-2x1, 4x1		„		
38	**21.02.2018**	Design of multiplexers-8x1, 16x1		„		
39	**22.02.2018**	Design of De-multiplexers		„		
40	**22.02.2018**	**Priority encoder**		„		
41	**23.02.2018**	Comparators		„		
42	**28.02.2018**	BCD to 7segment display		„		
		Sequential Logic Circuits:	**V**	Chalk & Board		
		Flip-Flops-Truth tables, Excitation tables:				
43	**01.03.2018**	S-R Latch, Flip-Flop, D Flip-Flop		„		
44	**01.03.2018**	J-K, T Flip-Flops		„		
45	**02.03.2018**	Conversion of Flip-Flops		„		
46	**07.03.2018**	Design of Ripple counters		„		
47	**08.03.2018**	**Design of synchronous counters:** 4-bit binary		„		
48	**08.03.2018**	Decade counter		„		
49	**09.03.2018**	Design of shift Registers		„		
50	**14.03.2018**	Design of buffer shift registers		„		
51	**15.03.2018**	Design of Bi-directional shift registers		„		
52	**15.03.2018**	Design of universal shift register		„		
53	**16.03.2018**	Design of Johnson & Ring counters.		„		

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